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PATENT APPLICATION
DOCKET NO.: 2789.2017-000

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JC978 U.S. PTO
09/862384
05/22/01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Ramin Farjad-Rad

Attorney's Docket No: 2789.2017-000

Title: LINEAR DATA RECOVERY PHASE DETECTOR

Date: 5-22-01

EXPRESS MAIL LABEL NO. EL760234109US

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This Information Disclosure Statement is submitted:

[ ] under 37 CFR 1.129(a), or
(First/Second submission after Final Rejection)

[X] under 37 CFR 1.97(b), or
(Within any one of the following time periods: three months of filing national application (other than a CPA) or date of entry of the national stage in an international application; or before the mailing date of a first office action on the merits in a non-provisional application, including a CPA, or a Request for Continued Examination).

[ ] under 37 CFR 1.97(c) together with either:

[ ] a Statement under 37 CFR 1.97(e), as checked below, or

[ ] a $180.00 fee under 37 CFR 1.17(p), or
(After the 37 CFR 1.97(b) time period, but before final action or notice of allowance, whichever occurs first)

[ ] under 37 CFR 1.97(d) together with:

[ ] a Statement under 37 CFR 1.97(e), as checked below, and

[ ] a $180.00 fee under 37 CFR 1.17(p), or
(Filed after final action or notice of allowance, whichever occurs first, but on or before payment of the issue fee)

[ ] under 37 CFR 1.97(i):
Applicant requests that the IDS and cited reference(s) be placed in the application filewrapper.
(Filed after payment of issue fee)

Statement Under 37 CFR 1.97(e)

[ ] Each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement; or

[ ] No item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned, after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of this Information Disclosure Statement.

Statement Under 37 CFR 1.704(d) (Patent Term Adjustment)
Applies to original applications (other than design) filed on or after May 29, 2000

[ ] Each item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in § 1.56(c) more than thirty days prior to the filing of the Information Disclosure Statement.

[X] Enclosed herewith is form PTO-1449:

[X] Copies of the cited references are enclosed.

[ ] Copies of cited references are enclosed except those entered in prior application, U.S. Application No. [ ], to which priority under 35 U.S.C. 120 is claimed. [The earlier application contains copies of the cited references.]

[ ] The listed references were cited in the enclosed International Search Report in a counterpart foreign application.

[ ] The "concise explanation" requirement (non-English references) for reference(s) [ ] under 37 CFR 1.98(a)(3) is satisfied by:

[ ] the explanation provided on the attached sheet.

[ ] the explanation provided in the Specification.

[ ] submission of the enclosed International Search Report.

[ ] the enclosed English language abstract.

[ ] Applicant requests that the following pending applications be considered:

Examiner's Initials

_____ U.S. Patent Application No. [ ], Publication No. [ ], Publication Date [ ], by [inventor(s)], filed [ ], Docket No.: [ ]

_____ U.S. Patent Application No. [ ], Publication No. [ ], Publication Date [ ], by [inventor(s)], filed [ ], Docket No.: [ ]

_____ U.S. Patent Application No. [ ], Publication No. [ ], Publication Date [ ], by [inventor(s)], filed [ ], Docket No.: [ ]

_____ _____
Examiner Date

[ ] A copy of each above-cited application, including the current claims, is enclosed.

[ ] A copy of each above-cited application, including the current claims, is enclosed, except those entered in prior application, U.S. Application No. [ ], to which priority under 35 U.S.C. 120 is claimed.

The Examiner is requested to return a copy of the above list of pending applications indicating which references were considered with the next office communication.

It is requested that the information disclosed herein be made of record in this application.

Method of payment:

[ ] A check for the fee noted above is enclosed, or the fee has been included in the check with the accompanying Reply. A copy of this Statement is enclosed.

[ ] Please charge Deposit Account 08-0380 in the amount of $[ ]. A copy of this Statement is enclosed.

[X] Please charge any deficiency in fees and credit any overpayment to Deposit Account 08-0380.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By _____
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Lexington, Massachusetts 02421-4799
Dated: 5/22/01

PTO-1449 REPRODUCED	ATTORNEY DOCKET NO. 2789.2017-000	APPLICATION NO.
INFORMATION DISCLOSURE CITATION IN AN APPLICATION	APPLICANT Ramin Farjad-Rad	
May 16, 2001	FILING DATE	GROUP
(Use several sheets if necessary)		

JC978 U.S. PTO 09/862384 05/22/01

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION YES	NO
	AL							
	AM							

OTHER DOCUMENTS ***(Including Author, Title, Date, Pertinent Pages, Etc.)***

W	AR	Lee, Thomas H., et al., *"A 155-MHZ Clock Recovery Delay - and Phase-Locked Loop,"* pp. 421-430, Reprinted from IEEE Journal of Solid-State Circuits, vol. SC-27, pp. 1736-1746, December 1992.
	AS	Soyuer, Mehmet, *"A Monolithic 2.3-Gb/s 100-mW Clock and Data Recovery Circuit in Silicon Bipolar Technology,"* pp. 450-453, Reprinted from IEEE Journal of Solid-State Circuits, vol. SC-28, pp. 1310-1313, December 1993.
	AT	Savoj, Jafar, et al., *"A 10-Gb/s CMOS Clock and Data Recovery Circuit,"* IEEE, pp. 136-139.
	AU	Poulton, John, et al., *"A Tracking Clock Recovery Receiver for 4Gb/s Signaling,"* pp. 157-169.
	AV	Hu, Timothy H., *"A Monolithic 480 Mb/s Parallel AGC/Decision/Clock-Recovery Circuit in 1.2-μm CMOS,"* pp. 437-443, Reprinted from IEEE Journal of Solid-State Circuits, vol. SC-28, pp. 1314-1320, December 1993.
	AW	Ishihara, Noboru, et al., *"A Monolithic 156 Mb/s Clock and Data Recovery PLL Circuit Using the Sample-and-Hold Technique,"* pp. 431-436, Reprinted from IEEE Journal of Solid-State Circuits, vol. SC-29, pp. 1566-1571, December 1994.
	AX	Farjad-Rad, Ramin, et al., *"A 0.3-μm CMOS 8-Gb/s 4-PAM Serial Link Transceiver,"* pp. 757-764.
	AY	Fiedler, Alan, et al., *"A 1.0625Gbps Transceiver with 2x-Oversampling and Transmit Signal Pre-Emphasis,"* IEEE, pp. 462-464.
	AZ	Thon, L., *"540Mhz 21 mW MDFE Equalizer and Detector in 0.25μm CMOS,"* IEEE.
	AR2	Dally, William J., *"Transmitter Equalization for 4Gb/s Signaling,"* pp. 29-38.

EXAMINER	DATE CONSIDERED
6/30/04	6/30/04